LESSON PLAN (SUMMER-2024)

Discipline:ETC	Semester:6th	Name of the Teaching Faculty: P.Bhawani
Subject: Control System	No of Days /per week class allotted:4	Semester From date: 16/01/2024 to 26/04/2024 No of Weeks:15
Week	**Class Day**	**Theory Topics**
1st	1st	1.1 Classification of Control system
	2nd	1.2 Open loop system & Closed loop system and its comparison
	3rd	1.3 Effects of Feed back
	4th	1.4 Standard test Signals(Step, Ramp, Parabolic, Impulse Functions)
2nd	1st	1.5 Servomechanism 1.6 Regulators (Regulating systems)
	2nd	2.1 Transfer Function of a system & Impulse response
	3rd	2.2 Properties,Advantages& Disadvantages of Transfer Function
	4th	2.3 Poles & Zeroes of transfer Function, 2.4 Representation of poles & Zero on the s-plane
3rd	1st	2.5 Simple problems of transfer function of network
	2nd	2.5 Simple problems of transfer function of network
	3rd	2.5 Simple problems of transfer function of network
	4th	2.5 Simple problems of transfer function of network
4th	1st	2.5 Simple problems of transfer function of network
	2nd	3.1 Components of Control System
	3rd	3.2 Potentiometer
	4th	3.2Synchros, 3.3 DC motors, AC Servomotors
5th	1st	3.4 Modelling of Electrical Systems(R, L, C, Analogous systems)
	2nd	3.4 Modelling of Electrical Systems(R, L, C, Analogous systems)
	3rd	4.1 Definition of Basic Elements of a Block Diagram
	4th	4.2 Canonical Form of Closed loop System
6th	1st	4.3 Rules for Block diagram Reduction,
	2nd	4.3 Rules for Block diagram Reduction,
	3rd	4.6 Basic Definition in SFG & properties
	4th	4.7 Mason's Gain formula, 4.8 Steps for solving Signal flow Graph
7th	1st	4.9 Simple problems in Signal flow graph for network
	2nd	4.9 Simple problems in Signal flow graph for network
	3rd	5.1 Definition of Time, Stability, steady-state response, accuracy, transient accuracy, In-sensitivity and robustness.
	4th	5.2 System Time Response
8th	1st	5.3 Analysis of Steady State Error
	2nd	5.4 Types of Input & Steady state Error(Step ,Ramp, Parabolic)
	3rd	5.5 Parameters of first order system & second-order systems
	4th	5.5 Parameters of first order system & second-order systems
9th	1st	5.6 Derivation of time response Specification (Delay time, Rise time)
	2nd	5.6 Derivation of time response Specification (Peak time,Setting time,Peak over shoot)
	3rd	6.1 Effect of parameter variation in Open loop System & Closed loop Systems
	4th	6.2 Introduction to Basic control Action
10th	1st	Basic modes of feedback control: proportional, integral and derivative
	2nd	6.3 Effect of feedback on overall gain, Stability
	3rd	6.4 Realisation of Controllers(P, PI) with OPAMP
	4th	6.4 Realisation of Controllers(PD,PID) with OPAMP
11th	1st	7.1 Effect of location of poles on stability
	2nd	7.2 RouthHurwitz stability criterion.
	3rd	7.3 Steps for Root locus method
	4th	7.4 Root locus method of design(Simple problem)

12th	1st	7.4 Root locus method of design(Simple problem)
	2nd	7.4 Root locus method of design(Simple problem)
	3rd	7.4 Root locus method of design(Simple problem)
	4th	7.4 Root locus method of design(Simple problem)
13th	1st	8.1 Frequencyresponse,Relationship between time & frequency response
	2nd	8.2 Methods of Frequency response, 8.3 Polar plots & steps for polar plot
	3rd	8.4 Bodes plot & steps for Bode plots
	4th	8.5 Stability in frequency domain, Gain Margin& Phase margin
14th	1st	8.6 Nyquist plots. Nyquiststability criterion.
	2nd	8.7 Simple problems as above
	3rd	8.7 Simple problems as above
	4th	9.1 Concepts of state, state variable, state model,
15th	1st	9.1 Concepts of state, state variable, state model,
	2nd	9.2 state modelsfor linear continuous time functions(Simple)
	3rd	9.2 state modelsfor linear continuous time functions(Simple)
	4th	9.2 state modelsfor linear continuous time functions(Simple)

Signature of the faculty

LESSON PLAN (SUMMER-2024)		
Discipline:IT	**Semester: 4th**	**Name of the Teaching Faculty: P BHAWANI**
Subject: Microprocessor & Microcontroller	**No of Days /per week class allotted: 5**	**Semister from date: 16/01/2024 to 26/04/2024** **No of weeks: 15**
Week	**Class Day**	**Theory Topics**
1st	1st	**Unit-1:Microprocessor (Architecture and Programming-8085-8-bit) (15)** 1.1 Introduction to Microprocessor and Microcomputer & distinguish between them.
	2nd	1.2 Concept of Address bus, Data bus, Control bus & System Bus
	3rd	1.3 General Bus structure Block diagram.
	4th	1.4 Basic Architecture of 8085 (8 bit) Microprocessor
	5th	1.4 Basic Architecture of 8085 (8 bit) Microprocessor
2nd	1st	1.4 Basic Architecture of 8085 (8 bit) Microprocessor
	2nd	1.5 Signal Description (Pin diagram) of 8085 Microprocessor
	3rd	1.5 Signal Description (Pin diagram) of 8085 Microprocessor
	4th	1.5 Signal Description (Pin diagram) of 8085 Microprocessor
	5th	1.6 Register Organizations,Distinguish between SPR & GPR
3rd	1st	Timing & Control Module
	2nd	1.7 Stack, Stack pointer &Stack top.
	3rd	1.7 Stack, Stack pointer &Stack top.
	4th	1.8 Interrupts:-8085 Interrupts, Masking of Interrupt(SIM,RIM)
	5th	1.8 Interrupts:-8085 Interrupts, Masking of Interrupt(SIM,RIM)
4th	1st	**Unit-2: Instruction Set and Assembly Language Programming (15)** 2.1 Addressing data & Differentiate between one-byte, two-byte &three-byte instructions with examples.
	2nd	2.2 Addressing modes in instructions with suitable examples.
	3rd	2.2 Addressing modes in instructions with suitable examples.
	4th	2.3 Instruction Set of 8085(Data Transfer, Arithmetic, Logical, Branching, Stack& I/O , Machine Control)
	5th	2.3 Instruction Set of 8085(Data Transfer, Arithmetic, Logical, Branching, Stack& I/O , Machine Control)
5th	1st	2.4 Simple Assembly Language Programming of 8085 2.4.1 Simple Addition & Subtraction
	2nd	2.4 Simple Assembly Language Programming of 8085 2.4.1 Simple Addition & Subtraction
	3rd	2.4.2 Logic Operations (AND, OR, Complement 1's & 2's) & Masking of bits
	4th	2.4.3 Counters & Time delay (Single Register, Register Pair, More than Two Register)
	5th	2.4.4 Looping, Counting & Indexing (Call/JMP etc).
6th	1st	2.4.5 Stack & Subroutine programes.
	2nd	2.4.6 Code conversion, BCD Arithmetic & 16 Bit data Operation, Block Transfer.
	3rd	2.4.7 Compare between two numbers
	4th	2.4.8 Array Handling (Largest number & smallest number in the array)
	5th	2.5 Memory & I/O Addressing,
7th	1st	**Unit-3: TIMING DIAGRAMS. (8)** 3.1 Define opcode, operand, T-State, Fetch cycle, Machine Cycle, Instruction cycle & discuss the concept of timing diagram.
	2nd	3.1 Define opcode, operand, T-State, Fetch cycle, Machine Cycle, Instruction cycle & discuss the concept of timing diagram.
	3rd	3.2 Draw timing diagram for memory read, memory write, I/O read, I/O write machine cycle.
	4th	3.2 Draw timing diagram for memory read, memory write,
	5th	3.2 Draw timing diagram for I/O read, I/O write machine cycle.
	1st	3.3 Draw a neat sketch for the timing diagram for 8085 instruction MOV instruction).

8th	2nd	3.3 Draw a neat sketch for the timing diagram for 8085 instruction MVI instruction).
	3rd	3.3 Draw a neat sketch for the timing diagram for 8085 instruction LDA instruction.
	4th	Unit-4 Microprocessor Based System Development Aids (10) 4.1 Concept of interfacing
	5th	4.2 Define Mapping &Data transfer mechanisms - Memory mapping & I/O Mapping
9th	1st	4.3 Concept of Memory Interfacing:- Interfacing EPROM & RAM Memories
	2nd	4.4 Concept of Address decoding for I/O devices
	3rd	4.5 Programmable Peripheral Interface: 8255
	4th	4.5 Programmable Peripheral Interface: 8255
	5th	4.6 ADC & DAC with Interfacing.
10th	1st	4.6 ADC & DAC with Interfacing.
	2nd	4.7 Interfacing Seven Segment Displays
	3rd	4.8 Generate square waves on all lines of 8255
	4th	4.9 Design Interface a traffic light control system using 8255.
	5th	4.9 Design Interface a traffic light control system using 8255.
11th	1st	4.10 Design interface for stepper motor control using 8255.
	2nd	4.11 Basic concept of other Interfacing DMA controller,USART
	3rd	**Unit-5 Microprocessor (Architecture and Programming-8086-16 bit) (12)** 5.1 Register Organisation of 8086
	4th	5.2 Internal architecture of 8086
	5th	5.2 Internal architecture of 8086
12th	1st	5.3 Signal Descriptionof 8086
	2nd	5.3 Signal Descriptionof 8086
	3rd	5.4 General Bus Operation& Physical Memory Organisation
	4th	5.5 MinimumMode&Timings, 5.6 Maximum Mode&Timings,
	5th	5.7 Interrupts and Interrupt Service Routines, Interrupt Cycle, Non-Maskable Interrupt, Maskable Interrupt
13th	1st	5.8 8086 Instruction Set & Programming: Addressing Modes, Instruction Set, Assembler Directives and Operators,
	2nd	5.9 Simple Assembly language programmingusing 8086 instructions.
	3rd	**Unit-6 Microcontroller (Architecture and Programming-8 bit) (15)** 6.1 Distinguish between Microprocessor & Microcontroller
	4th	6.2 8 bit & 16 bit microcontroller 6.3 CISC & RISC processor
	5th	6.4 Architectureof8051Microcontroller
14th	1st	6.4 Architectureof8051Microcontroller
	2nd	6.5 Signal Descriptionof8051Microcontrollers
	3rd	6.6 Memory Organisation-RAM structure, SFR
	4th	6.7 Registers,timers,interruptsof8051Microcontrollers
	5th	6.8 Addressing Modes of 8051
15th	1st	6.9 Simple 8051 Assembly Language ProgrammingArithmetic & Logic Instructions , JUMP, LOOP, CALL Instructions, I/O Port Programming
	2nd	6.9 Simple 8051 Assembly Language ProgrammingArithmetic & Logic Instructions , JUMP, LOOP, CALL Instructions, I/O Port Programming
	3rd	6.10 Interrupts, Timer & Counters
	4th	6.11 Serial Communication
	5th	6.12 Microcontroller Interrupts and Interfacing to 8255

Signature of the faculty